OIP. CS-00-025

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To: Commissioner of Patents and Trademarks Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572 20 McIntosh Drive Poughkeepsie, N.Y. 12603 JUL 2 0 2001 TC 1700

Subject:

Serial No. 09/845,480 04/30/01

S.F. Quek, T.C. Ang, Y.C. Wong, S.Y. Long

DOUBLE-LAYERED LOW DIELECTRIC CONSTANT DIELECTRIC DUAL DAMASCENE METHOD

Grp. Art Unit: 1765

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,083,822 to Lee, "Fabrication Process for Copper Structures", discloses a dual damascene method using a thin silicon nitride etch stop layer.

U.S. Patent 6,025,259 to Yu et al., "Dual Damascene Process Using High Selectivity Boundary Layers", discloses a dual damascene method with etch stop layers.

In Chang et al., <u>ULSI Technology</u>, The McGraw Hill Companies, Inc., NY, NY, c. 1996, pp. 444-445, discusses the damascene or dual damascene process.

- U.S. Patent 6,004,883 to Yu et al., "Dual Damascene Patterned Conductor Layer Formation Method Without Etch Stop Layer", discloses a dual damascene method without an etch stop layer.
- U.S. Patent 6,071,809 to Zhao, "Methods for Forming High-Performing Dual-Damascene Interconnect Structures", discusses a method using an etch stop layer.
- U.S. Patent 5,635,423 to Huang et al., "Simplified Dual Damascene Process for Multi-Level Metallization and Interconnection Structure", teaches various methods of forming a dual damascene opening.
- U.S. Patent 5,741,626 to Jain et al., "Method for Forming a Dielectric Tantalum Nitride Layer as an Anti-reflective Coating (ARC)", discloses a dual damascene process using a tantalum nitride etch stop layer.

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The following two U.S. Patents disclose a double mask self-aligned process using a silicon nitride etch sotp layer:

- 1) U.S. Patent 5,935,762 to Dai et al., "Two-Layered TSI Process for Dual Damascene Patterning".
- 2) U.S. Patent 5,877,076 to Dai, "Opposed Two-Layered Photoresist Process for Dual Damascene Patterning".

Sincerely,

George O. Saile, Reg. No. 19572